IN THE CLAIMS:

Please cancel Claims 1 to 27 and substitute new claims 28 to 49 as follows:

1. - 27. (Cancelled).

28. (New) An information processing apparatus comprising:

processing means; and

mode setting means for setting a mode of a memory,

wherein said processing means sets said mode setting means in an enable state, and commands the memory to issue therefrom a power saving mode transfer instruction for setting said processing means in a power saving mode, and

wherein said mode setting means sets the memory in a power saving mode in accordance with a signal which relates to the setting of said processing means in the power saving mode and inputted to said mode setting means while said mode setting means is in the enabled state.

29. (New) An information processing apparatus according to claim 28, further comprising detecting means for detecting an instruction fetch transfer for the power saving mode transfer instruction and outputting the signal in accordance with detection of the instruction fetch transfer for the power saving mode transfer instruction, and wherein said mode setting means sets the memory in the power saving mode in accordance with the signal inputted from said detecting means while said mode setting means is in the enabled state.

30. (New) An information processing apparatus according to claim 28, wherein if said processing means detects an interruption for returning to the normal operation mode from the power saving mode, said processing means returns a normal operation mode from the power saving mode and invalidates the signal relating to the setting of said processing means in the power saving mode, and

wherein said mode setting means sets the memory in a normal operation mode in accordance with invalidation of the signal relating to the setting of said processing means in the power saving mode.

31. (New) An information processing apparatus according to claim 28, wherein said processing means outputs the signal for notifying said mode setting means that said processing means is transferred to the power saving mode, and

wherein said mode setting means sets the memory in the power saving mode in accordance with the signal inputted from said processing means while said mode setting means is in the enabled state.

32. (New) An information processing apparatus according to claim 28, wherein said mode setting means sets the memory in the power saving mode after an end of memory transfer in progress.

33. (New) An information processing apparatus comprising:

processing means; and

mode transfer means for transferring a mode of a memory,

wherein said processing means sets said mode transfer means in a waiting state, and executes a power saving mode transfer instruction for setting said processing means in a power saving mode, and

wherein said mode transfer means transfers the memory to a power saving mode after the end of the waiting state.

34. (New) An information processing apparatus according to claim 33, wherein said mode transfer means supplies the memory with a predetermined signal to transfer the memory to the power saving mode from a normal operation mode.

35. (New) An information processing apparatus according to claim 33, wherein said mode transfer means transfers the memory to a normal operation mode in accordance with an interruption for returning said processing means to a normal operation mode from the power saving mode.

36. (New) An information processing apparatus according to claim 33, wherein said processing means sets a time of period of the waiting state, and said mode transfer means transfers the memory to the power saving mode after a lapse of the time of period of the waiting state.

37. (New) An information processing apparatus according to claim 33, wherein said processing means instructs said mode transfer means to start counting a lapse of a time period of the waiting state.

38. (New) An information processing apparatus according to claim 33, wherein said mode transfer means transfers the memory to the power saving mode after an end of memory transfer in progress.

39. (New) A power saving controlling method for a processor and a memory, the method comprising:

an enable state setting step of setting a memory controller for controlling the memory in an enable state;

a requesting step of commanding the memory to issue therefrom a power saving mode transfer instruction for setting the processor in a power saving mode; and

a power saving mode setting step of setting the memory in a power saving mode in accordance with a signal which relates to the setting of the processor in the power saving mode and inputted to the memory controller while memory controller is in the enabled state.

40. (New) A power saving controlling method according to claim 39, further comprising:

a detecting step of detecting an instruction fetch transfer for the power saving mode transfer instruction; and

an outputting step of outputting the signal in accordance with detection of the instruction fetch transfer for the power saving mode transfer instruction,

wherein the memory is set in the power saving mode at said enable state setting step in accordance with the signal outputted in said detecting step while the memory controller is in the enabled state.

41. (New) A power saving controlling method according to claim 39, further comprising:

a returning step of returning the processor to a normal operation mode from the power saving mode in accordance with an interruption;

an invalidating step of invalidating the signal relating to the setting of the processor in the power saving mode in accordance with the returning to the normal operation mode of the processor; and

a returning step of returning the memory to a normal operation mode in accordance with invalidation of the signal relating to the setting of the processor in the power saving mode.

42. (New) A power saving controlling method according to claim 39, further comprising an outputting step of outputting the signal for notifying memory controller that the processor is transferred to the power saving mode, and

wherein the memory is set in the power saving mode at said power saving mode setting step in accordance with the signal outputted at said outputting step while said mode setting means is in the enabled state.

43. (New) A power saving controlling method according to claim 39, wherein the memory is set to the power saving mode at said power saving mode setting step after an end of memory transfer in progress.

44. (Currently Amended) A power saving controlling method for a processor and a memory, the method comprising:

a setting step of setting a memory controller for controlling the memory in a waiting state;

an executing step of executing a power saving mode transfer instruction for setting the processor in a power saving mode; and

a transferring step of transferring the memory to a power saving mode after the end of the waiting state.

45. (New) A power saving controlling method according to claim 44, wherein said transferring step supplies the memory with a predetermined signal to transfer the memory to the power saving mode from a normal operation mode.

46. (New) A power saving controlling method according to claim 44, further comprising a returning step of returning the memory to a normal operation mode in accordance with an interruption for returning the processor to a normal operation mode from the power saving mode.

47. (New) A power saving controlling method according to claim 44, further comprising a setting step of setting a time of period of the waiting state, and wherein the memory is transferred to the power saving mode in said transferring step after a lapse of the time of period of the waiting state.

48. (New) A power saving controlling method according to claim 44, further comprising an instructing step of instructing the memory controller to start counting a lapse of a time period of the waiting state.

49. (New) A power saving controlling method according to claim 44, wherein the memory is transferred to the power saving mode after an end of memory transfer in progress.